AMENDMENT TO THE CLAIMS:

This listing of claims will replace all prior versions, and listing, of claims in the application.

Listing of Claims:

1. (Currently Amended) A thin film transistor array panel comprising:

a first conductive layer formed on an insulating substrate;

a gate insulating layer on the first conductive layer;

a semiconductor layer on the gate insulating layer;

a second conductive layer formed at least in part on the semiconductor layer and including a data line, ~~and~~ a drain electrode ~~separated from each other~~and a data pad located at an end of the data line, the second conductive layer including a lower film of barrier metal and an upper film of Al or Al alloy;

a passivation layer covering the semiconductor layer; and

a third conductive layer formed on the passivation~~second conductive~~ layer and contacting the second conductive layer, the third conductive layer including a pixel electrode and a pad electrode,

wherein at least an edge of the upper film lies on the lower film such that the lower film includes a first portion and a second portion exposed out of the upper film of the drain electrode and the data pad respectively, and the pixel electrode and the pad electrode, respectively,~~third conductive layer~~ contacts the first portion and the second portion of the lower film;~~, and~~

the edge of the upper film of the drain electrode around the first portion is separated from the pixel electrode, and

the edge of the upper film of the data pad around the second portion is separated from the pad electrode.

~~at least one portion of a boundary of the semiconductor layer substantially coincides with a boundary of the lower film.~~

2. (Currently Amended) The thin film transistor array panel of claim 1, wherein an edge of the upper film of the drain electrode traverses the lower film of the drain electrode.

3. (Currently Amended) The thin film transistor array panel of claim 1, wherein the passivation layer has a contact hole exposing the first portion of the lower film of the drain electrode~~layer~~ at least in part,

at least a portion of the pixel electrode is located on the passivation layer, and

the at least an edge of the upper film of the drain electrode does not coincide with a boundary of the contact hole.

4. (Currently Amended) The thin film transistor array panel of claim 3, wherein the passivation layer contacts the lower film of the drain electrode near the contact hole.

5. (Currently Amended) The thin film transistor array panel of claim 1, wherein the lower film of the drain electrode, the data pad or both comprises Cr, Mo or Mo alloy.

6. (Original) The thin film transistor array panel of claim 1, further comprising an ohmic contact interposed between the semiconductor layer and the second conductive layer.

7. (Original) The thin film transistor array panel of claim 6, wherein the ohmic contact has substantially the same planar shape as the second conductive layer.

8. (Canceled)

9. (Original) The thin film transistor array panel of claim 1, wherein the third conductive layer comprises ITO or IZO.

10. (Cancelled)

11. (Currently Amended) The thin film transistor array panel of claim 10, wherein the passivation layer has a first contact hole for contact between the drain electrode and the pixel electrode, a second contact hole exposing a portion of the first conductive layer, and a third contact hole exposing a portion of the data line, and the third conductive layer comprises a first

contact assistant contacting the first conductive layer through the second contact hole and a second contact assistant contacting the data line through the third contact hole.

12. (Original) The thin film transistor array panel of claim 1, wherein the first portion of the second conductive layer has unevenness.

13. – 19. (Canceled)

20. (Currently Amended) A thin film transistor array panel comprising:

a gate conductive layer formed on an insulating substrate;

a gate insulating layer on the gate conductive layer;

a semiconductor layer on the gate insulating layer;

a data conductive layer formed at least in part on the semiconductor layer and including a data line and a drain electrode separated from each other;

a passivation layer covering the semiconductor layer; and

a pixel electrode contacting the drain electrode,

wherein at least one portion of the semiconductor layer is formed along with the data line, and

a boundary of the semiconductor layer is exposed out of the data line except for places near the drain electrode and an end portion of the data line.

21. (Original) The thin film transistor array panel of claim 20, wherein the data conductive layer has a multilayered structure including a lower film and an upper film, and the lower film and the upper film have different shapes.

22. (Original) The thin film transistor array panel of claim 21, wherein the lower film comprises a barrier metal and the upper film comprises Al or Al alloy.

23. (Original) The thin film transistor array panel of claim 20, wherein the data line has an edge substantially parallel to the semiconductor layer, the edge of the data line either placed on the semiconductor layer or coinciding with an edge of the semiconductor layer.

24. (Original) The thin film transistor array panel of claim 23, wherein the pixel electrode has an edge overlapping the gate conductive layer, the data conductive layer, or the semiconductor layer.

25. (Original) The thin film transistor array panel of claim 20, further comprising an ohmic contact interposed between the semiconductor layer and the data conductive layer and having substantially the same planar shape as the data conductive layer.

26. (Original) The thin film transistor array panel of claim 20, wherein a lateral side of the data conductive layer is tapered.

27. (Original) The thin film transistor array panel of claim 20, wherein the passivation layer has a first contact hole for contact between the drain electrode and the pixel electrode, a second contact hole exposing a portion of the gate conductive layer, and a third contact hole exposing a portion of the data line, and further comprising:

a first contact assistant contacting the gate conductive layer through the second contact hole and a second contact assistant contacting the data line through the third contact hole, the first and the second contact including the same layer as the pixel electrode.

28. (Original) The thin film transistor array panel of claim 27, wherein the passivation layer contacts the lower film near the first and the second contact holes.

29. (Original) The thin film transistor array panel of claim 20, wherein a portion of the drain electrode contacting the pixel electrode has unevenness.

30. – 35. (Canceled)